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A Simple Staircase Modulation for A Cascaded H-bridge Multilevel Inverter

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Abstract: This paper proposes a novel simple staircase modulation to obtain reasonable performance of an output voltage for a cascaded H-Bridge multilevel inverter. The motivation of the proposed algorithm is that the inverter phase voltage intersects with an original sinusoidal waveform at equal points in the y-axis. This modulation technique can calculate the independent switching angles more simply than the traditional method, which employed Fourier's series analysis, and can be applied to all kinds of multilevel inverters. In this paper, for the sake of validation, the technique was applied to a cascaded H-bridge inverter with unequal DC sources. Then, it was applied to the seventh, ninth, eleventh, and twenty-seventh levels of the multilevel inverter. In addition, pulse width modulation techniques used in this type of multilevel inverter are complicated. The PSIM software program was used for all simulation examples, and its results are consistent with the experimental results.

Keywords: *Multilevel inverter*; *cascaded H-bridge inverter; staircase modulation; pulse width modulation; nearest level control.*

1. INTRODUCTION

Multilevel inverters are currently used instead of two-level inverters, especially in high-voltage applications. Low-voltage switches are used in multilevel inverters while high-voltage switches are used in two-level inverters. Low-voltage switches are used in multilevel inverters, because, the response is faster, smaller, and are cheaper. The ability to withstand high voltages increases when switches are connected in a series. Multilevel inverters provide better sinusoidal voltage waveform compared to the two-level inverters because their output voltage contained more than two voltage levels.

There are different types of multilevel inverters; the cascaded H-bridge inverters, the diode clamp inverters, the flying capacitor inverters, and the series-parallel H-bridge inverters [1-6]. Cascaded H-bridge multilevel inverters (CHB-MLIs) are sub-divided into two types: equal DC source and unequal DC source. Strategies that are used in multilevel inverters are classified according to their switching frequencies [7] as shown in **Fig.1**. A CHB-MLI is used for all aspects of life application, such as residential, commercial and industrial, transportation, utility systems, aerospace and telecommunications systems [8, 9].

A CHB-MLI acquires the following features, which makes it favourable for many applications: simple to use in commercial units; it has availability good improved systems; has minimaldv/dt; and has lesser voltage total harmonic distortion (THD). It produces high AC voltage without requiring power electronics devices in series. A CHB-MLI produces minimal common mode voltage and, more importantly, if the distance between the converter and the drive is long, there will be no over voltage on the AC drive terminal [10-12]. The main disadvantage of a CHB-MLI is that it requires separate DC sources, i.e., DC link capacitors for each cell, which leads to high component count.

The staircase selective harmonic elimination (SHE) method was proposed in 1973 by Patel and Hof[13].This method was founded on Fourier's series calculation of phase voltage of cascaded H-bridge inverter. The main disadvantage of this method is that the number of equations, the number of variables, and the order of The equations increase as the number of inverters increase. Thus, finding solutions for these equations would become complicated, take a long time to process, and often include modern numerical methods algorithms, which make the calculation difficult to reach owing to the limits of existing computer numerical software programs [14-19]. Pulse width modulation techniques that are used in CHB-MLIs with unequal DC sources are difficult and complicated [20, 21].

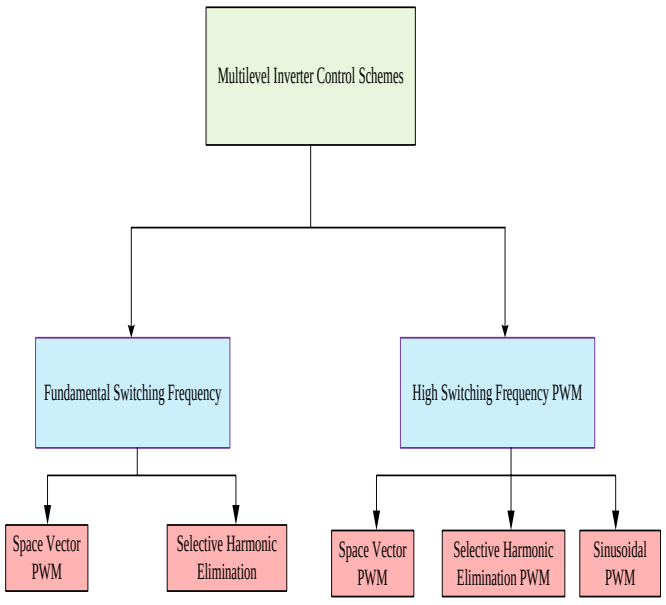


Fig.1. Classification of multilevel inverter modulation techniques

In this research, a simple staircase modulation technique has been used to obtain lower THD in a CHB-MLI. The contribution of this work is that the proposed staircase modulation technique calculates the independent switching angles more simply than the traditional methods.

Section 4 explains the main differences between the simple staircase modulations used in this paper and nearest level controls (NLCs).

2. CASCADED H-BRIDGE MULTILEVEL INVERTER

1.1 Cascaded H-Bridge with Equal DC Source

The circuit configuration of single-phase L levels CHB-MLI with equal DC sources is shown in **Fig. 2.** The relationship between levels of inverters and the number of cells (Single-phase H-bridge) is given by:

$$L = (2C + 1) \quad (1)$$

where C is the number of H-bridge cells. The levels L of the inverter are constantly odd numbers for the CHB-MLI [22, 23]. The phase voltage of the CHB-MLI is:

$$V_{ph} = V_{c1} + V_{c2} + V_{c3} + \cdots + V_{CN} \quad (2)$$

where V_{CN} is the output voltage of H-bridge cells. The voltage levels of L inverters are in range

$\left(-\left(\frac{L-1}{2}\right)V_{dc}, -\left(\frac{L-2}{2}\right)V_{dc}, \cdots, 0, \cdots, \left(\frac{L-2}{2}\right)V_{dc}, \left(\frac{L-1}{2}\right)V_{dc}\right)$[24, 25]. For seven levels, the levels of the CHB-MLI are$(-3V_{dc}, -2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}, 3V_{dc})$.

The total number of devices (IGBT) used in the CHB-MLI per phase can be given by:

$$N_{SW} = 2(L - 1) \quad (3)$$

1.2 Cascaded H-Bridge with Unequal DC Source

The DC input sources of the CHB-MLI transistor cells were illustrated in Section 2.1 above are all equals. For a CHB-MLI with an unequal DC source, the number of cells can be reduced by adding more DC sources for the power transistors cells. The last level of a cascaded H-bridge with an unequal DC source is given by:

$$\boldsymbol{M = 3^C} \quad (4)$$

The total number of devices (IGBT) used in a CHB-MLI with an unequal DC source can be given by:

$$N_{SW} = 4C \quad (5)$$

Moreover, the maximum output voltage of a CHB-MLI with an unequal DC source can be given by:

$$V_{o,max} = \left(\frac{3^C-1}{2}\right)V_{dc} \quad (6)$$

Table 1 summarizes the number of cells, number of levels, number of devices, and the maximum output voltage of a CHB-MLI with unequal DC sources. **Fig.3**. shows four configurations of this type of CHB-MLI.

Table 1. Summary of cascaded H-bridge inverter with unequal DC sources

Number of cells	Number of levels available	Number of devices	Maximum output voltage
2	5,7,9	8	$4V_{dc}$
3	7,9,11,…,27	12	$13V_{dc}$
4	9,11,13,…,81	16	$40V_{dc}$
5	11,13,15,…,243	20	$121V_{dc}$

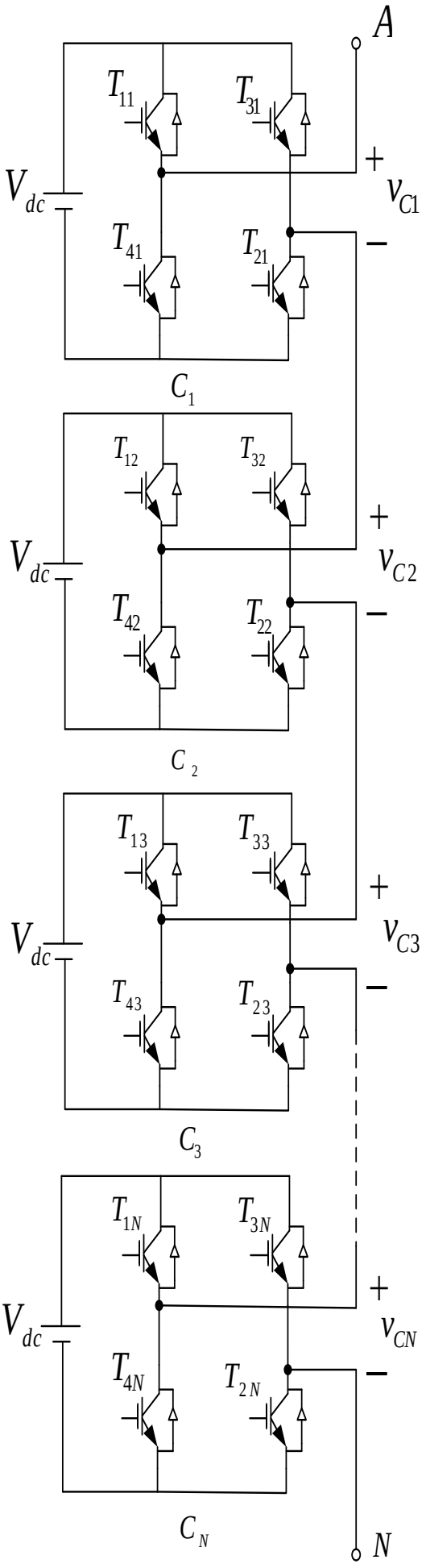


Fig. 2. Configuration of L levels of cascaded H-bridge inverter

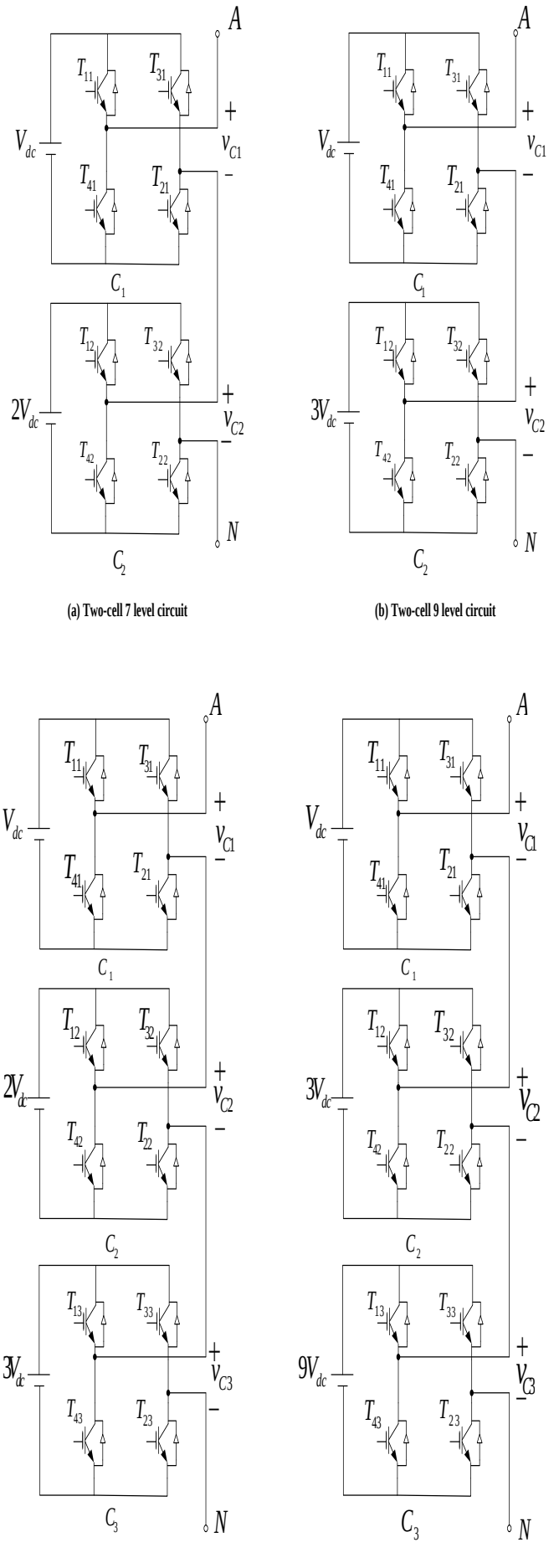


Fig.3. Per-phase configuration of CHB-MLI with unequal DC sources

3. SIMPLE STAIRCASE MODULATION TECHNIQUE

The principle of the method used in this paper is shown in **Fig.4** [26]. The inverter phase voltage is created by a seven-level inverter.

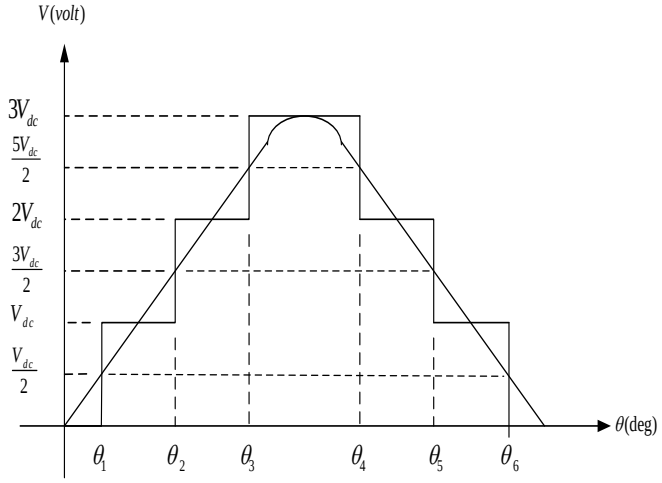


Fig.4. Simple staircase modulation of a seven-level inverter

The method's algorithm relies on the fact that the inverter phase voltage intersects with an original sinusoidal waveform at equal points on the y-axis. It can be clearly seen from **Fig. 4** that these equal points are$\left(\frac{V_{dc}}{2}, V_{dc}, \frac{3V_{dc}}{2}, 2V_{dc}, \frac{5V_{dc}}{2}, 3V_{dc}\right)$. Thus angles θ_1 to $\theta_6$can be calculated by:

$$\frac{V_{dc}}{2} = 3V_{dc}sin(\theta_1) \Rightarrow \theta_1 = \sin^{-1}\left(\frac{1}{6}\right) \quad (7)$$

$$\frac{3V_{dc}}{2} = 3V_{dc}sin(\theta_2) \Rightarrow \theta_2 = \sin^{-1}\left(\frac{1}{2}\right) \quad (8)$$

$$\frac{5V_{dc}}{2} = 3V_{dc}sin(\theta_3) \Rightarrow \theta_3 = \sin^{-1}\left(\frac{5}{6}\right) \quad (9)$$

$$\theta_4 = \pi - \theta_3, \theta_5 = \pi - \theta_2, \theta_6 = \pi - \theta_1 \quad (10)$$

In general, for any multilevel inverter, the angles between intervals 0 to π/2 can be given by:

$$\theta_{n+1} = \sin^{-1}\left(\frac{2n+1}{2M}\right) \quad (11)$$

where n = 0,1,2,…,M-1 , $M = \frac{L-1}{2}$, and L is the level of the inverter.The angles between intervals π/2 to π are calculated from complementary angles similar to Equation 10.

4. NEAREST LEVEL CONTROL METHOD

The nearest level control (NLC) method is shown in **Fig. 5**. The main difference between the simple staircase modulations proposed in this paper and NLC is that a sinusoidal reference voltage Vref is matched with the DC voltage levels of the inverter in the NLC. The nearest level to the reference voltage is selected. The output voltage V will be a staircase voltage with a minimum possible error with respect to the reference voltage V^*[27-32]. The nearest output voltage level V is calculated by:

$$V = V_{dc}round(V^*/V_{dc}) \quad (12)$$

While in a simple staircase modulation the angles can be calculated directly from Equation 11, and it does not need comparison between the original sinusoidal and level voltage.

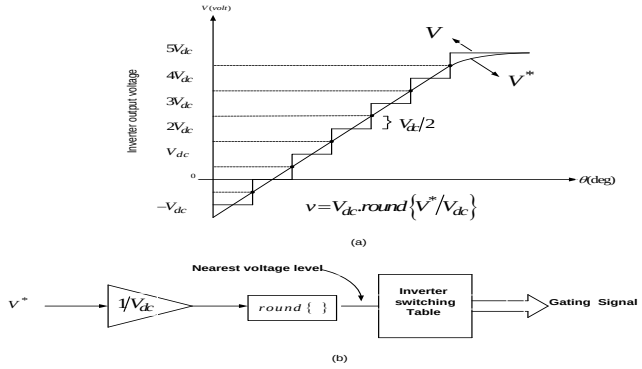


Fig. 5. Nearest level selection (a) waveform synthesis and (b) control diagram.

5. ILLUSTRATED EXAMPLES

In this paper, simple staircase modulation was applied to four topologies of CHB-MLI with unequal DC sources shown in **Fig. 4**. In the seven-level circuit, the DC voltages for cell C_1 and cell C_2 are V_{dc} and $2V_{dc}$, respectively. The two inverter cells produce seven voltages.

Levels$(-3V_{dc}, -2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}, 3V_{dc})$.**Table 2** illustrates the relationship between the voltage level and their corresponding states of transistor switches. The six angles of simple staircase modulation are calculated using Equation10 and 11.

$$\theta_1 = sin^{-1}(1/6) = 9.594068227^{\circ}$$
$$\theta_2 = sin^{-1}(1/2) = 30^{\circ}$$
$$\theta_3 = sin^{-1}(5/6) = 56.44269024^{\circ}$$
$$\theta_4 = \pi - \theta_3 = 123.55730976^{\circ}$$
$$\theta_5 = \pi - \theta_2 = 150^{\circ}$$
$$\theta_6 = \pi - \theta_1 = 170.405931773^{\circ}$$

It is worth mentioning that all simulation examples are carried out using the PSIM software program.

Fig.6 demonstrates the phase voltage and fast Fourier transform (FFT) of a seven-level inverter with unequal DC sources. The angle of the staircase modulation is based on the Fourier series for CHB inverters because of its unique structure [33, 34].

Table 3 compares a simple staircase modulation and staircase modulation, which was calculated by the Fourier's series for a CHB seven-level inverter. It can be seen from the table that the simple staircase modulation has a better THD. On the other hand, the simple staircase modulation can be used to calculate the angles of a nine-level inverter with two cells, an eleven-level inverter with three cells, and a twenty-seven-level inverter with three cells as shown in **Fig. 4** (b), (c), and (d), respectively.

Table 2 phase voltage and switching state of seven level inverter

State of switches								Cell voltages		Phase voltage
T_{11}	T_{31}	T_{41}	T_{21}	T_{12}	T_{32}	T_{42}	T_{22}	V_{c1}	V_{c2}	V_{ph}
0	0	1	1	0	0	1	1	0	0	0
1	0	0	1	0	0	1	1	V_{dc}	0	V_{dc}
0	0	1`	1	1	0	0	1	0	$2V_{dc}$	$2V_{dc}$
1	0	0	1	1	0	0	1	V_{dc}	$2V_{dc}$	$3V_{dc}$
0	0	1	1	1	0	0	1	0	$2V_{dc}$	$2V_{dc}$
1	0	0	1	0	0	1	1	V_{dc}	0	V_{dc}
0	0	1	1	0	0	1	1	0	0	0
0	1	1	0	0	0	1	1	$-V_{dc}$	0	$-V_{dc}$
0	0	1	1	0	1	1	0	0	-2Vdc	$-2V_{dc}$
0	1	1	0	0	1	1	0	$-V_{dc}$	-2Vdc	$-3V_{dc}$
0	0	1	1	0	1	1	0	0	$-2V_{dc}$	$-2V_{dc}$
0	1	1	0	0	0	1	1	$-V_{dc}$	0	$-V_{dc}$
0	0	1	1	0	0	1	1	0	0	0

All results are shown in **Table 4**. The THD of the nine-level inverter with two cells, the eleven-level inverter with three cells, and the twenty-seven-level inverter with three cells was calculated using the PSIM software program.

Table 5 illustrates the relationship between the voltage level and its corresponding states of transistor switches for a nine-level inverter with unequal DC sources.

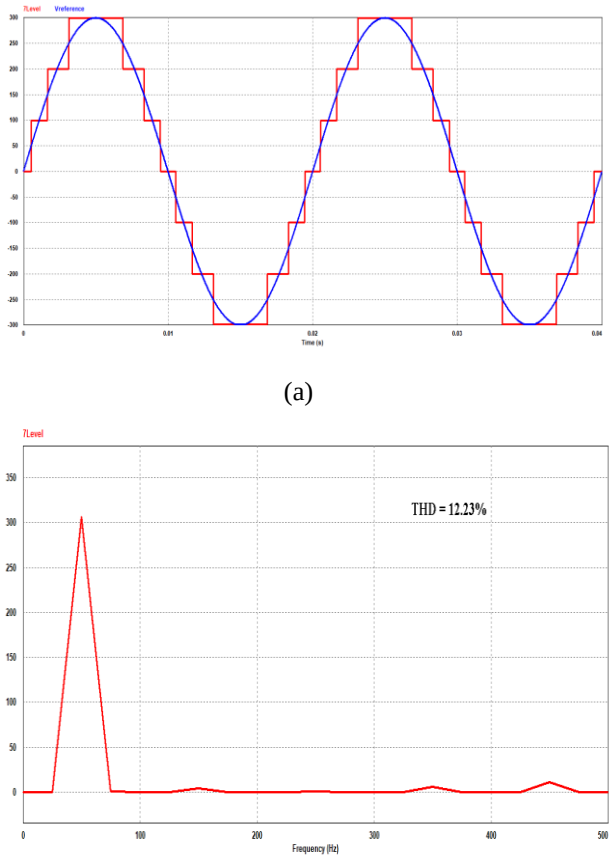


Fig. 6. (a) Phase voltage of seven level and original sinusoidal (b) FFT of phase voltage

Table 3. Comparison between simple staircase and staircase modulation based on Fourier's series for seven-level inverter

Angle	Simple staircase	Staircase based on Fourier series
θ_1	9.594068227°	11.504°
θ_2	30°	28.717°
θ_3	56.44269024°	57.106°
THD	12.230855%	12.5%

Table 4. Angles and THD for level-9, level-11 and level-27 CHB –MLI with unequal dc sources (all angles in degree unit)

$0 \le \theta_1 \le /\pi/2$	Level-9	Level-11	Level-27
θ_1	7.180755781	5.739170477	2.204227504
θ_2	22.02431284	17.45760312	6.625809565
θ_3	38.68218745	30	11.0874892
θ_4	61.04497563	44.427004	15.61849828
θ_5	-	64.15806724	20.25224674
θ_6	-	-	25.02899949
θ_7	-	-	30
θ_8	-	-	35.23441798
θ_9	-	-	40.83221703
θ_{10}	-	-	46.9509202
θ_{11}	-	-	53.87107253
θ_{12}	-	-	62.2042275
θ_{13}	-	-	74.05763139
THD	9.3716042%	7.5855813%	3.0215694%

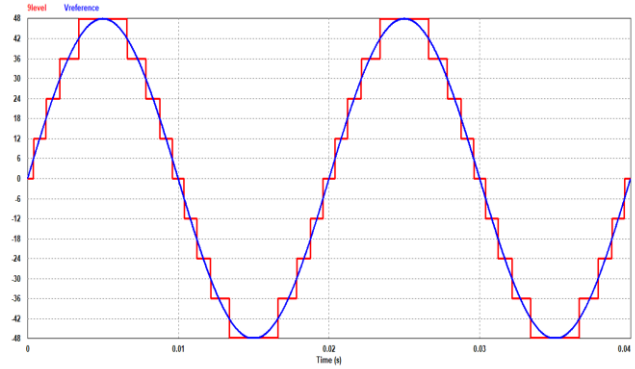
Fig.7. shows the PSIM simulation of the phase voltage of the nine-level, inverter with unequal DC sources. The phase voltage of an eleven-level and twenty seven-level inverter will be simulated in the same way using angles calculated in Table 4.

6. EXPERIMENTAL RESULTS

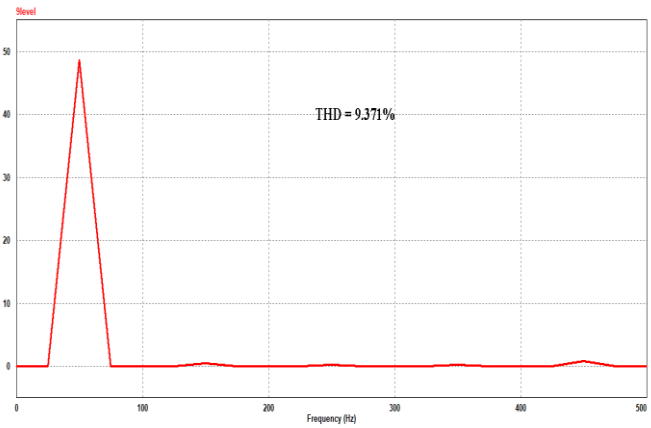
The practical implementation of a cascaded multilevel inverter with staircase modulation requires designing of a circuit that can produce gating signals for each level at accurate angles. Although there are other methods to realize a staircase multilevel inverter, the proposed method is based on calculating the accurate angles for each level, making the implantation less complicated by utilizing the high-speed processing capability and high timing accuracy of the microcontroller.

Table 5. Phase voltage and switching state of nine level inverter

State of switches								Cell voltages		Phase voltage
T_{11}	T_{31}	T_{41}	T_{21}	T_{12}	T_{32}	T_{42}	T_{22}	V_{c1}	V_{c2}	V_{ph}
0	0	1	1	0	0	1	1	0	0	0
1	0	0	1	0	0	1	1	V_{dc}	0	V_{dc}
0	1	1`	0	1	0	0	1	$-V_{dc}$	$3V_{dc}$	$2V_{dc}$
0	0	1	1	1	0	0	1	0	$3V_{dc}$	$3V_{dc}$
1	0	0	1	1	0	0	1	V_{dc}	$3V_{dc}$	$4V_{dc}$
0	0	1	1	1	0	0	1	0	$3V_{dc}$	$3V_{dc}$
0	1	1	0	1	0	0	1	$-V_{dc}$	$3V_{dc}$	$2V_{dc}$
1	0	0	1	0	0	1	1	V_{dc}	0	V_{dc}
0	0	1	1	0	0	1	1	0	0	0
0	1	1	0	0	0	1	1	$-V_{dc}$	0	$-V_{dc}$
1	0	0	1	0	1	1	0	V_{dc}	$-3V_{dc}$	$-2V_{dc}$
0	0	1	1	0	1	1	0	0	$-3V_{dc}$	$-3V_{dc}$
0	1	1	0	0	1	1	0	$-V_{dc}$	$-3V_{dc}$	$-4V_{dc}$



(a)



(b)

Fig. 7. (a) Phase voltage of 9-level and original sinusoidal (b) FFT of phase voltage

The nine-level CHB inverter with unequal DC sources was first implemented with Proteus simulation software. Following that, the circuit was realized with actual components as shown in **Fig. 8**.

Additionally, a microcontroller (PIC16F877A) was used to produce the accurate gating signals at each calculated angle by using the timer and interrupting modules of the microcontroller to generate the gating signal at pre-calculated times related to the calculated angles.

The MOSFT Driver (IR2112) was utilized to amplify or boost the 5V gating signal from the microcontroller to a level that is required by the MOSFET power transistor.

The MOSFET Power transistor (IRF450) was also used as main building block of the H-bridge inverter cells. DC power supply was used to provide the required power of the circuit items. As aforementioned, the microcontroller used micro C language. The voltage phase of the experimental result of a nine-level CHBI is shown in **Fig. 9**.

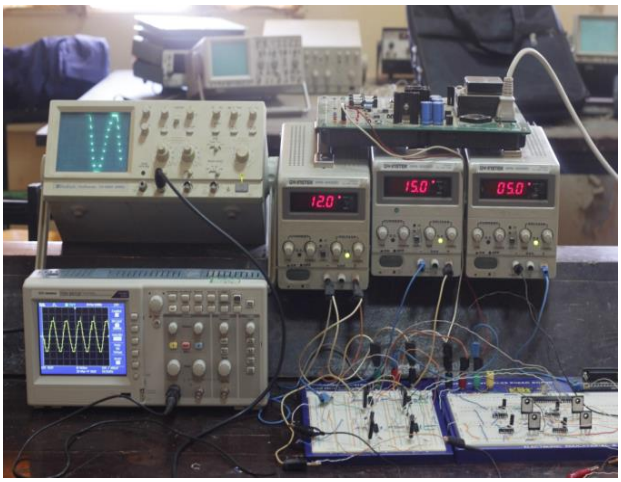


Fig. 8. Experimental prototype of a nine levels CHBI with unequal DC sources

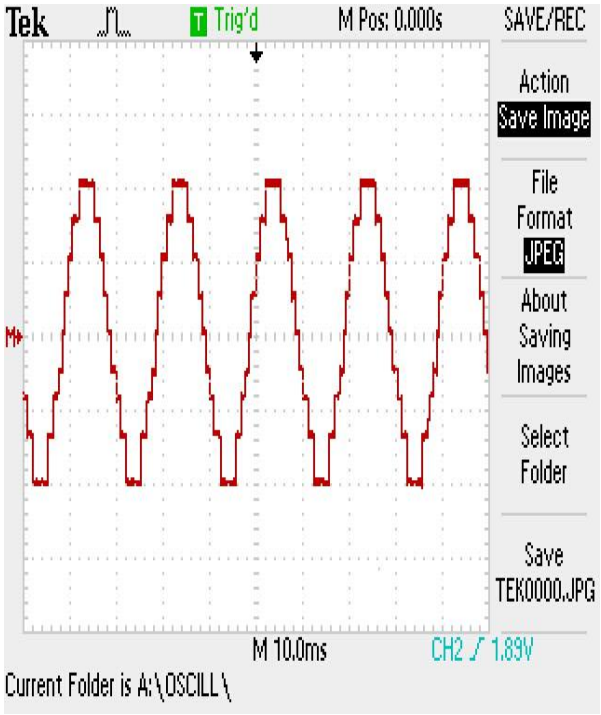


Fig. 9. Voltage phase of experimental result of a nine level CHB with unequal DC source

7. CONCLUSIONS

In this paper, a simple staircase modulation for multilevel inverters was discussed and was applied to CHB-MLI with unequal DC sources. The proposed simple staircase modulation scheme avoided implementation complexities. All the switching angles can be computed using the method proposed in this paper to make implementation less complicated by utilizing the high-speed processing capability and high timing accuracy of the microcontroller. All IGBT of the inverter operates at the fundamental frequency. This algorithm has been applied to seven, nine, eleven and twenty-seven-level CHB-MLI with an unequal DC source. The output phase voltage of the inverters does not contain the higher order harmonics and has a low THD. The main difference between the algorithm proposed in this paper and the nearest level control was discussed. In this paper, the experimental results for a nine-level inverter with unequal DC were matched with the computer simulation results.

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